Q.P. Code: 19EC4202 R19

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

M.Tech I Year II Semester Regular Examinations October-2020

DIGITAL IC DESIGN

(Embedded Systems)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1.	**a**	Draw the circuit for NMOS inverter and explain its operation.	**8M**
	b	List the advantages of dynamic logic over static CMOS logic.	**4M**
		OR	
2.	**a**	Describe how the clock skew problem is overcomes in domino CMOS circuits.	**6M**
	b	Draw the circuit topology and explain the operation of CMOS domino logic.	**6M**

UNIT-II

3.	**a**	Illustrate the method of logical effort for transistor sizing.	**6M**
	b	Draw the circuit for 4 transistors SRAM and explain its working.	**6M**
		OR	
4.	**a**	Explain the logical effort of two – input NAND and NOR gates with neat circuit diagram.	**6M**
	b	In what way the DRAMs differ from SRAMs?	**6M**

UNIT-III

5.	**a**	Design NAND gate in BiCMOS logic.	**6M**
	b	What is dynamic behavior of BiCMOS logic? Explain in detail with neat sketches.	**6M**
		OR	
6.	**a**	Give the schematic diagram of different Bi-CMOS inverters. Explain its operation.	**6M**
	b	List the advantages and disadvantages of BiCMOS.	**6M**

UNIT-IV

7.	**a**	What is the need for design rules? Explain.	**4M**
	b	Explain the CMOS based design rules with neat sketches.	**8M**
		OR	
8.		Write about:	
	a.	Area capacitance.	**6M**
	b.	Drive large capacitive load.	**6M**

UNIT-V

9.	**a**	How to design the ALU sub-system? Give the process.	**6M**
	b	Construct 4-bit SISO and explain its operations.	**6M**
		OR	
10.	**a**	Explain what subsystem design process is.	**6M**
	b	Design the sub-system Serial-Parallel Multiplier.	**6M**

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